WHAT IS CLAIMED IS:

1. A clamp circuit integrated in a semiconductor integrated circuit with an input terminal and configured to clamp a voltage inputted to the input terminal of the semiconductor integrated circuit, said clamp circuit comprising:

a first transistor having a gate, a source, a drain connected to the gate and a conductivity type, said first transistor being configured to shift a target clamp voltage applied on the source by a gate-source voltage to output the shifted target clamp voltage, said gate-source voltage representing a voltage between the gate and the source of the first transistor;

a buffer circuit having an output terminal and connected to the first transistor, said buffer circuit being configured to input the shifted voltage outputted from the first transistor and output a reference voltage according to the inputted shifted voltage; and

a second transistor having a gate, a source, a drain and a conductivity type which is the same as the conductivity type of the first transistor, said gate being connected to the output terminal of the buffer circuit, said source being connected to the input terminal of the first transistor.

2. The clamp circuit according to claim 1, wherein said gate and drain of the second transistor are connected to each other.

3. The clamp circuit according to claim 1, wherein said first and

second transistors have substrate voltages and source voltages, respectively, and each of said substrate voltages of the first and second transistors is set to substantially equal to each of the source voltages thereof.

4. The clamp circuit according to claim 1, wherein each of said first and second transistors has a same size and a same connection structure regarding each drain, source and back gate.

5. The clamp circuit according to claim 1, wherein said drain and gate of the first transistor is connected to a power supply line of the semiconductor integrated circuit

6. The clamp circuit according to claim 1, wherein said semiconductor integrated circuit is mounted on a substrate, a current regulating element is connected to the input terminal of the semiconductor integrated circuit and mounted at an exterior thereof on the substrate, and said source of the second transistor is connected to the current regulating element through the input terminal.

7. The clamp circuit according to claim 1, wherein said first and second transistors have different sizes, respectively.

8. The clamp circuit according to claim 1, further comprising a constant current circuit connected to the drain and gate of the first transistor.

9. The clamp circuit according to claim 1, wherein said buffer circuit comprises an operational amplifier having a reverse input terminal, a non-reverse input terminal and an output terminal, and configured as a voltage follower so that the reverse input terminal is connected to the output terminal, and said non-reverse input terminal is connected to the drain and gate of the first transistor.

10. A clamp circuit integrated in a semiconductor integrated circuit with an input terminal and configured to clamp a voltage inputted to the input terminal of the semiconductor integrated circuit, said clamp circuit comprising:

a first transistor having a base, an emitter, a collector connected to the base and a type of junction, said first transistor being configured to shift a target clamp voltage applied on the emitter by a base-emitter voltage to output the shifted target clamp voltage, said base-emitter voltage representing a voltage between the base and the emitter of the first transistor;

a buffer circuit having an output terminal and connected to the first transistor, said buffer circuit being configured to input the shifted voltage outputted from the first transistor and output a reference voltage according to the inputted shifted voltage; and

a second transistor having a base, an emitter, a collector and a type of junction which is the same as the type of junction of the first transistor, said base being connected to the output terminal of the buffer circuit, said emitter being connected to the input terminal of the first transistor.

11. The clamp circuit according to claim 10, wherein said base and collector of the second transistor are connected to each other.

12. The clamp circuit according to claim 10, wherein said first and second transistors have substrate voltages and source voltages, respectively, and each of said substrate voltages of the first and second transistors is set to substantially equal to each of the source voltages thereof.

13. The clamp circuit according to claim 10, wherein each of said first and second transistors has a same size.

14. The clamp circuit according to claim 10, wherein said collector and base of the first transistor is connected to a power supply line of the semiconductor integrated circuit

15. The clamp circuit according to claim 10, wherein said semiconductor integrated circuit is mounted on a substrate, a current regulating element is connected to the input terminal of the semiconductor integrated circuit and mounted at an exterior thereof on the substrate, and said collector of the second transistor is connected to the current regulating element through the input terminal.

16. The clamp circuit according to claim 10, wherein said first and second transistors have different sizes, respectively.

17. The clamp circuit according to claim 10, further comprising a constant current circuit connected to the collector and base of the first transistor.

18. The clamp circuit according to claim 10, wherein said buffer circuit comprises an operational amplifier having a reverse input terminal, a non-reverse input terminal and an output terminal, and configured as a voltage follower so that the reverse input terminal is connected to the output terminal, and said non-reverse input terminal is connected to the collector and base of the first transistor.